# SAINT WIEN DIGITAL COUNTER

H7N- P1/4

#### TYPE H7N- DIN 72x72, 72x144 PROGRAMMABLE DIGITAL COUNTER PANEL CUT 68x68,H68xW139mm ■ FEATURES

- 1 INCORPORATE AN EXCLUSIVE ONE-CHIP MICROPROCESSOR,
- MAXIMUM PROGRAMMABLE 448 DIFFERENT SPECIFICATIONS.
  (2 COUNTING DIRECTIONS, 4 COUNTING SPEEDS, 3 OPERATION MODES, 7 COUNTING VERSIONS)
- 3 OUTSTANDING NOISE IMMUNITY WITH SCHMITT TRIGGER CIRCUIT APPLIED TO ALLINPUT TERMINALS FOR WIDE NOISE MARGIN AND NOISE SUPPRESSOR INSERTED IN LSI WHERE REQUIRED.
- 4 ALL INPUTS AND OUTPUTS ISOLATED WITH PHOTO ISOLATOR.
- 5 30 CPS SOFTWARE DEBOUNCE FOR CONTACT/SWITCH INPUT. 3000 CPS FOR VOLTAGE(SENSOR OR ENCODER) INPUT.
- 6 UP, DOWN COUNT AND REVERSIBLE VERSIONS AVAILABLE.
- 7 H OPERATION MODE FOR HIGH LIMIT OPERATION.
- 8 0.05~10S ADJUSTABLE FOR AUTO RESET CONTROL.
- 9 SINGLE OR DOUBLE STEP PRESET AVAILABLE.
- 10 LEADING ZERO BLANK AVAILABLE UPON REQUEST.
- 11 EEPROM BACKUP FOR MEMORY PROTECTION AVAILABLE.
- 12 MINUS SIGN OR BORROW INDICATION AVAILABLE
- 13 7 COUNTINGVERSIONS PROVIDE PHASE DIFFERENCE IN, INDIVIDUAL IN, GATE IN & COMMAND IN.
- 14 CYCLE(x1) OR EDGE(x2, x4) COUNTING SELECTABLE FOR PHASE DIFFERENCE INPUT REVERSIBLE VERSIONS.
- 15 8 OPERATION MODES FOR AUTO/MAN RESET. OPERATION MODES OF CRPQH FOR AUTO RESET, NFK FOR MAN RESET.

AVAILABLE TYPES
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H7N-

Classsification		Digital Counter						
Counting versions		UO, DOWN, REVERSIBLE COUNT						
Preset			Yes	Yes	Not			
Backup memory			Not	Yes	Yes			
Display			Yes	Yes	Yes			
Type Nos. of Digits & steps of preset S=Single Preset D=Double Preset	2D	S	H7N-2D	H7N-2DM				
		D	H7N-2D2D	H7N-2D2DM				
	3D	S	H7N-3D	H7N-3DM				
		D	H7N-3D3D	H7-3D3DM				
	4D	S	H7N-4D	H7N-4DM	H7N-4M			
		D	H7N-4D2D*	H7N-4D2DM*				
		D	H7N-4D4D	H7N-4D4DM				
	5D	S	H7N-5D	H7N-5DM	H7N-5M			
		D	H7N-5D2D*	H7N-5D2DM*				
		D	H7N-5D3D*	H7N-5D3DM*				
		D	H7N-5D5D-L	H7N-5D5DM-L				
	6D	S	H7N-6D	H7N-6DM	H7N-6M			
		D	H7N-6D2D*	H7N-6D2DM*				
		D	H7N-6D6D-L	H7N-6D6DM-L				
	7D	S	H7N-7D	H7N-7DM	H7N-7M			
		D	H7N-7D7D-L	H7N-7D7DM-L				
	8D	S	H7N-8D-L	H7N-8DM-L	H7N-8M-L			
		D	H7N-8D8D-L	H7N-8D8DM-L				

ORDER INFORMATIONS



Switch location at:

S is Section & Total/Bach counter same input

TS is Output of Section counter to Batch counter

T is Section & Total/batch counter separate input

Note: Above table, the types with mark of "\*" are DOWN count preset, suffix "-L" is case H72xW144mm 1. Standard: SINGLE COUNTER, 2~8 digits, single or double preset or no preset.

The preset code switch at right hand side is preset 2, left hand side is preset 1

The preset value should be always preset 1 greater than preset 2. The output of preset 2 is prior to preset 1

2. Special: TWIN COUNTER, 2~8 digits 2 counters (Section + Total/Batch) combination



### SPECIFICATIONS

- 1. Rate voltage: Nominal voltage 110/220VAC 50/60Hz (P1,P2=110V, P1,P2=220V)
- 2. Operating voltage: 85~115% of rated voltage

3. Power consumption: 3~5VA

- 4. Count & Gate & Reset input:
- A.. Contact/SW input: Connect +12VDC by short or open to input
- B. Solid state voltage input: [H]=6~30VDC,[L]=0~2VDC, Impedance=4.7Kohm
- 5. Maximum counting speeds of CP1, CP2 for input signal ON/OFF ratio=1:1

- C. U/D A; CP1 count in. CP2 command, CP2 [H]=-, CP2[L]=+ ......3000 cps
- D. U/D B; Individual count in. CP1 in=+, CP2 in=-.....3000 cps
- E. U/D C; Phase difference in, cycle count x1.....1000 cps
- F. U/D D; Phase difference in, edge count x2......1000 cps
- G. U/D E; Phase difference in, edge count x4......750 cps

6. Reset system: A. Power off reset: mini off time 0.5S. Reset time following signal application 0.5S B. External & MANual reset: reset time 0.5S. Reset time following signal application 0.5S

- C. AUTOmatic reset: internal reset by each operation mode C, R, K, P, Q, H.
- 7. Control output: A. Single preset (72x72, 72x144): Contact output SPDTx1 & voltage output (VOUT+12V)
  - B. Double preset (72x72): Contact output SPST-NOx2 (P4,5=#1, P6,12=#2)
  - C: Double preset (72x144): Contact output SPDTx2 & voltage output (VOUT+12V)
  - Contact rating:3A250VAC P.F.=1.0
- Solid state voltage output Vout=12VDC, output impedance 4.7Kohm
- 8. Power source for external sensor: 12VDC+-10%, 50mA

#### **PROGRAMMING OF SPECIFICATIONS** DIP SW/PIN POSITION: $\bullet$ = UP $\uparrow$ (0), $\odot$ = DOWN $\downarrow$ (1)

Specifications	$\downarrow$ DIP SW No. $\rightarrow$	1	2	3	4	5	6	7	8	9
Counting direction	UP	0								
	DOWN	•								
Maximum	30/30		•	•						
Counting	3K/30		0	•						
	3K/3K		0	0	1					
	30/3K		•	0						
Operation	N-Latch				0	0	0			
modes	F-Overflow				•	0	0			
	C-Recycle				0	•	0			
	R-Recycle				•	•	0			
	K-Overflow				0	0	•			
	P-Recycle				•	0	•			
	Q-Recycle				0	•	•			
	H-High limit				•	•	•			
Counting	CP1 in, CP2 gate							0	0	
versions	CP2 in, CP1 gate							0	•	С
	U/D A, CP2 H=- L=+							0	•	
	U/D B, Individual							0	0	С
	U/D C, Phase in x1							•	0	С
	U/D B, Phase in x2							•	•	С
	U/D C, Phase in x4							•	$\circ$	

Step 1: Removal of switch cover Remove the SW cover in the Manner shown in the photograph.

🗕 Ta 🕳 🖛 Tb 🕳

Input signal Ta=Tb≧Ta min=Tb min



With a screw driver raise and remove the switch cover at lower portion of the front.

screw ariver switch cover Step 2: Selection of specifications. By changing the respective pin's position of the DIP SW inside the cover. Various functional specification can be selected as shown in left table.

- Step 3: Indication of specification items. Select the appropriate rating label
- Note: Please manual reset after changing the pin's position, otherwise will work on previous functions.





Note:

\*Time chart is for O/P 1 of single counter. O/P 2 will be reset slave to O/P 1. \*Above chart for counter with minus [-] sign, except [K mode] is borrow.

U: Count up, from 0 to set value [n].

D: Count down, from set value [n] to 0.

[n]: Set value

[t]: Output holding time (one shot time) of 0.05S to 5S adjustable.

## COUNTING VERSIONS

[DESCRIPTION IS FOR UP COUNT PRESET DIP SW №.1=1↓ (○DOWN)]

- 1. CP1 IN, CP2 GATE [H]=INHIBIT...**Fig.1** CP1 count in, counter stops counting and hold display while [H] applying to CP2.
- CP2 IN, CP1 GATE [L]=INHIBIT...Fig.2 CP2 count in, counter counts only the CP1 is [H], stops counting while CP1 is [L].
- U/D A, CP2 command. H]=-, [L]=+...Fig.3 CP1 is count in, CP2 commands the counting Direction. CP2:[H] count down, [L] count up.
- U/D B, individual input. CP1=+, CP2=-...Fig.4 CP1 input cause increment. CP2 input cause decrement.
- U/D C, PHASE DIFFERENCE INPUTx1...Fig.5 CP1, CP2 be phase difference of 90. CP1, CP2 completes 1 cycle cause 1 increment or 1 decrement

- N: Display & O/P latched while the Counter is up
- F: Display overflow but O/P is latched while the counter is up
- C: Display & counter reset to count, but O/P latched while counter is up. O/P reset after timing [t].
- R: Display, counter & O/P is latched while counter is up. But all reset to count after timing [t].
- K: Display & counter overflow, O/P is latched while counter is up. O/P reset after timing [t].
- P: Display & O/P latched, counter reset to count while is up. O/P reset, display update after [t].
- Q: Display & counter overflow, O/P is latched while counter is up. But all reset after timing [t].
- H: Display& counter overflow, O/P is latched while counter equal or greater than set [n]. But O/P reset when counter smaller than set [n]



- U/D D, PHASE DIFFERENCE INPUTx2...Fig. 6 CP1, CP2 be phase difference of 90. CP1, CP2 completes 1 cycle cause 2 increment or decrement
- 7. U/D E, PHASE DIFFERENCE INPUTx4...Fig. 7 CP1, CP2 be phase difference of 90. CP1, CP2 completes 1 cycle cause 4 increment or decrement

OV RESET CP2

7 8

1

AC110V-

OV RESET

1 2 3

7 8

AC110V

(+)c

CP1 count input signal voltage

(—)

Fig.5

+E1

{-

+F (V)-

(-)

+E2

R1

Trt

Tr

AC220V

(+)

CP2 count input signal voltage

-AC220V



Fig.6

contact and solid-state input signals

Fig.12 Simultaneous application of input signals from one contact to multiple counters